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56 List of documents cited in the preliminary research report :
*Refer to end of present document*

*60 References to other related* National documents

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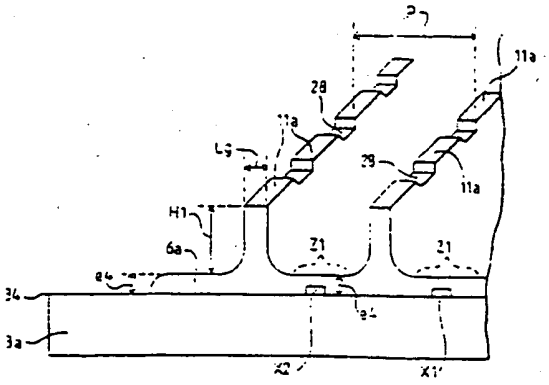
# 54 PROCESS FOR PRODUCING A DIELECTRIC LAYER INCLUDING RELIEF PATTERNS, ON A PLASMA PANEL PLATE

57 The present invention relates to a process for the fabrication, on a plasma panel sheet (3a), of a dielectric layer (6a) including relief patterns (11a).

Conforming to the invention, a vitreous layer is produced on a plasma panel plate (3a); a mold (M1) carrying patterns (B1,B2) in relief is applied on the vitreous layer (Vt), then the plate (3a) and the mold (M1) are heated until a flow effect is obtained in the vitreous layer (Vt) which causes the latter to conform to the shape of the mold.

The process of the invention thus permits the production, simultaneously and with improved qualities in relation to the prior art, of a dielectric layer (6a) bearing patterns such as, for example, barrier ribs (11a).

The invention is especially applicable in plasma panels of the alternative type.



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# PROCESS FOR PRODUCING A DIELECTRIC LAYER WITH RELIEF PATTERNS, ON A PLASMA PANEL

The present invention relates to a process for the fabrication on a plasma panel of a dielectric layer including patterns in relief. The invention finds an especially interesting application in plasma panels of the alternative type.

The plasma panels (shortened to "PDP" in the course of the description) are image visualization [display]* screens of the "flat screen" type, operating on the principle of a discharge in gases.

The PDP's generally include two insulating plates, each carrying one or more systems of electrodes, and defining between them a space filled with gas. The plates are assembled in such a way that the electrode systems are orthogonal. Each intersection of electrodes defines a cell with a corresponding gaseous space, a gaseous space in which an electrical discharge is produced with each activation of the cell.

Figure 1 represents, by way of example in a partial and simplified form, a standard structure of an alternative color PDP. It should be noted that there are different types of alternative PDP's, among which, for example, can be mentioned : those of the type using only two crossed electrodes to define and command a cell, as described particularly in a French patent published under the number 2 417 848 ; or even those of the type called "of coplanar structure", in which the structure and operation are described for example

* translator's note: square brackets [. . .] indicate alternative translation.

in the documentation of European patent EP-A-0.135.382. The alternative PDP's have one common characteristic, which is that of presenting during operation an internal memory effect, due to the fact that their electrodes are insulated from the gas and from the discharge by a layer of a dielectric material.

In the example of figure 1, the PDP is of the type with two crossed electrodes defining a cell. It contains two substrates or plates [tiles] 2, 3, of which one is a plate in front of 2, that is, that the plate that is on the side of the observer (not shown) ; this plate carries a first system of electrodes called "row electrodes", of which only 3 electrodes Y1, Y2, Y3 are shown. The row electrodes Y1 to Y3 are covered with a layer 5 of a dielectric material.

The second plate 3 forms the rear plate, opposite the observer ; it carried a second system of electrodes called "column electrodes", of which only 5 electrodes X1 to X5 are shown. The two plates 2, 3, are of the same material, generally of glass. These two plates 3, 3 are designed to be assembled with respect to each other in such a manner that the system of rows and columns of electrodes are orthogonal with respect to each other.

On the rear plate 3, the column electrodes X1 to X5 are arranged according to a step P, understood for example as between 100 μm and 500 μm according to the definition of the image. They are also covered with a layer 6 of a dielectric material, currently having a thickness e1 on the order of 20 μm to 30 μm. In the example shown, the dielectric layer 6 is itself covered by layers of phosphorescent materials forming bands [strips] 7, 8, 9, corresponding respectively for example to the colors green, red and blue. The rear plate 3 includes in addition a system of barriers 11, parallel to the column electrodes X1 to X5 as well as to the phosphor bands 7 to 9. These barriers 11 are arranged between adjacent phosphor bands in such a way as to separate them.

The PDP is formed after the assembly of the front and rear plates 2, 3, an assembly that creates an array of cells C1 to Cn. The cells are thus

as confinement, which relates to the insulation of the cells with respect to the other cells.

These different conditions are difficult to obtain with the standard methods of fabrication.

Figure 2 represents a barrier created in the classic way, by superposed layers : a plate 20 carries electrodes 21 , themselves covered with a dielectric layer 22 ; a barrier 23 is formed on the layer 22, by a number N of successive serigraphic operations, each producing a layer Cs1, . . ., CsN ; the number N may be understood for example as between 10 and 20 as a function of the height H1 to be attained.

A disadvantage in this method lies in the high number of serigraphic operations required to obtain the height H1. Another disadvantage is in the irregular profile of the edges of the barrier 23, which results from the impossibility of a perfect superposition of the successive layers Cs1 to CsN. Another disadvantage, finally, is that the height of the barrier is difficult to obtain with all the precision required, as the different layers Cs1 to Csn do not have a uniform thickness.

Another standard method of producing the barriers utilizes sanding operations (not shown). It consists of protecting the zones designed to constitute the barriers by masking and then by sanding to remove the material fron the non-protected zones. One of the weaknesses of this method is that the geometry of the barriers is limited, notably the edges are of necessity completely vertical and do not favor the luminescent yield. Another disadvantage lies in the risk of degrading the underlying dielectric layer during the sanding operation, which demands that a large number of especially punitive precautions be taken. Finally, a serious disadvantage in this method is that it produces large quantities of sand contaminated by the heavy metals contained in the layers subjected to sanding, which must therefore be re-treated [recycled].

The present invention proposes a process for creating a PDP plate, in a way that is simple and free of the defects and disadvantages mentioned

above, [and] simultaneously, a dielectric layer and the relief patterns such as for example the barrier system described earlier.

According to the invention, a process for producing a dielectric layer including relief patterns on a plasma panel plate, consisting of depositing a layer containing a glass frit on the plate, then vitrifying this layer which is then called a vitreous [glassy] layer", characterized in that [the process] consists of then pressing a mold bearing the relief patterns onto the vitreous layer , and of heating the unit formed by the mold and the plate carrying the vitreous layer to the point of obtaining a flow [ creep] effect in the vitreous layer which brings about the conformation of the vitreous layer to the shape of the mold.

By the term "relief pattern" we intend to define, with respect to the surface of the dielectric layer, the elevated elements forming bosses or projections as the barriers 11 , with the hollows [forming] the resists Ep1 to Epn, for example.

The invention will be better understood in reading the following description, given by way of non-restrictive example, with reference to the attached figures, among which :

- figure 1 already described, represents a color plasma panel of a standard structure ;
- figure 2 represents the fabrication of a barrier shown in figure 1 by a process of the prior art;
- figure 3 illustrates a first step in the process of the invention ;
- figure 4 represents the use of a mold in a succeeding step of the process according to the invention ;
- figure 5 represents a dielectric layer obtained according to the process of the invention ;
- figure 6 illustrates the production of a dielectric layer by the process of the invention, on a pre-existing dielectric layer.

Figure 3 is a partial representation of a plate 3a intended for example to constitute a rear PDP plate similar to the rear plate 3 shown in

(through incorporation of titanium in its composition), so as to form a white background in a PDP plate designed to direct the light towards the front ; the flow characteristics of such a dielectric are quite mediocre, and this initial layer would therefore not be affected by the treatment necessary to obtain the dielectric layer of the invention.

# CLAIMS

1. Process for producing a dielectric layer (6a) inclidung relief patterns (11a) , on a plasma panel plate (3a), consisting of depositing on the plate (3a) a layer (Ci) containing a frit of glass, then of vitrifying this layer which then becomes a vitreous layer (Vt), characterized in that it consists next of pressing onto this vitreous layer a mold (M1) bearing the relief patterns (11a) and of heating the assembly shaped by the mold (M1) and the plate (3a) carrying the vitreous layer (Vt), until a flow effect is obtained in the vitreous layer (Vt) that causes the latter to conform to the shape of the mold (M1) and to constitute the dielectric layer (6a) and the patterns (11a).

2. Process according to Claim 1, wherein the relief patterns are of barriers (11a) of the carrier barrier type fulfilling a spacer function.

3. Process according to one of the preceding claims, wherein the relief patterns are barriers (11a) of the type fulfilling a confinement function.

4. Process according to one of the preceding claims, wherein the process consists of pressing the mold (M1) onto the vitreous layer (Vt) with a pneumatic pressure exerted on the mold (M1) and the plate (3a).

5. Process according to one of Claims 1 to 4, wherein the process consists of installing a partial vacuum between the mold (M1) and the plate (3a) in order to press the mold (M1) onto the vitreous layer (Vt).

6. Process according to one of the preceding claims, wherein the pressure of the mold (M1) on the vitreous layer (Vt) is less than about $9.10^{4}$Pa.

7 Process according to one of the preceding claims, wherein the dielectric layer (6a) obtained has a thickness (e4) resulting from a thickness (e3) produced in the vitreous layer (Vt).

8. Process according to one of the preceding claims, wherein the process consists of forming the dielectric layer (6a) containing the patterns (11a) on a layer referred to as initial (31) , already produced on the plate (3a).

9. Process according to the preceding claim, wherein the initial layer (31) is a dielectric layer whose softening temperature is higher than the temperature towhich the vitreous layer (Vt) is subjected in order to obtain its flow.

10. Process according to one of Claims 8 or 9, wherein the initial layer (31) is white.

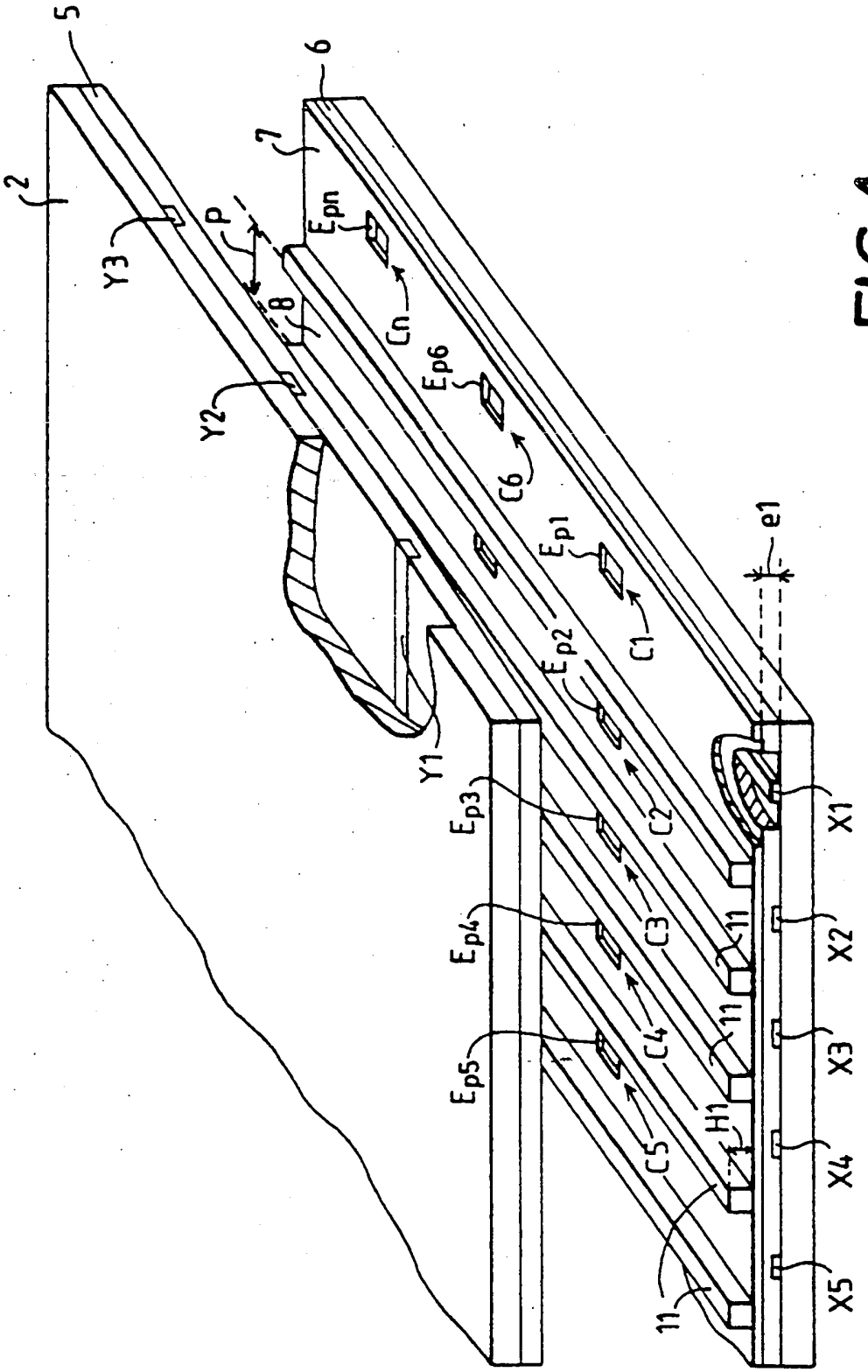
11. Process according to one of the preceding claims, wherein the mold (M1) is made of a metal plate whose face (32) carries the patterns (B1, B2) to be molded.

12. Process according to one of Claims 1 to 10, wherein the mold (M1) includes a glass substrate (SM).

13. Process according to the preceding Claim, wherein the glass substrate (SM) carries a metallic deposit (Dm) on one face (32), on which the patterns (B1, B2) to be molded have been produced .

14. Plasma panel plate obtained by the operation of the process following one of claims 1 to 13, including at least one system of electrodes (X1, X2), a dielectric layer (6a), barriers (11a), is characterized in that the dielectric layer (6a) and the barriers (11a) are comprised of the same layer (Vt) of a vitrified material.

15. Plasma panel plate according to Claim 14, wherein the dielectric layer (6a) and the barriers (11a) are obtained by a molding operation.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2
Y3
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Y2
Ep6
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C1
e1
Ep2
Y1
Ep3
C2
X1
Ep4
C3
11
X2
11
Ep5
C4
X3
H1
C5
X4
11
X5

FIG.1

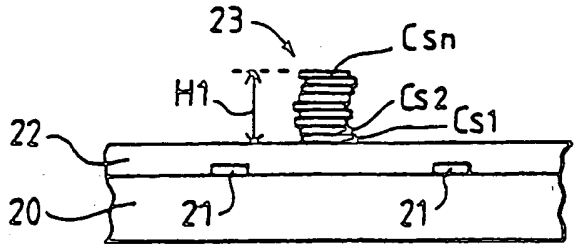



FIG.2

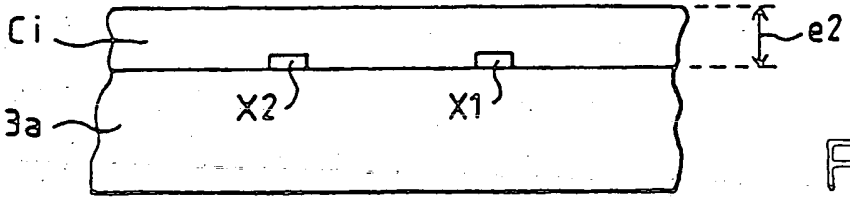



FIG.3

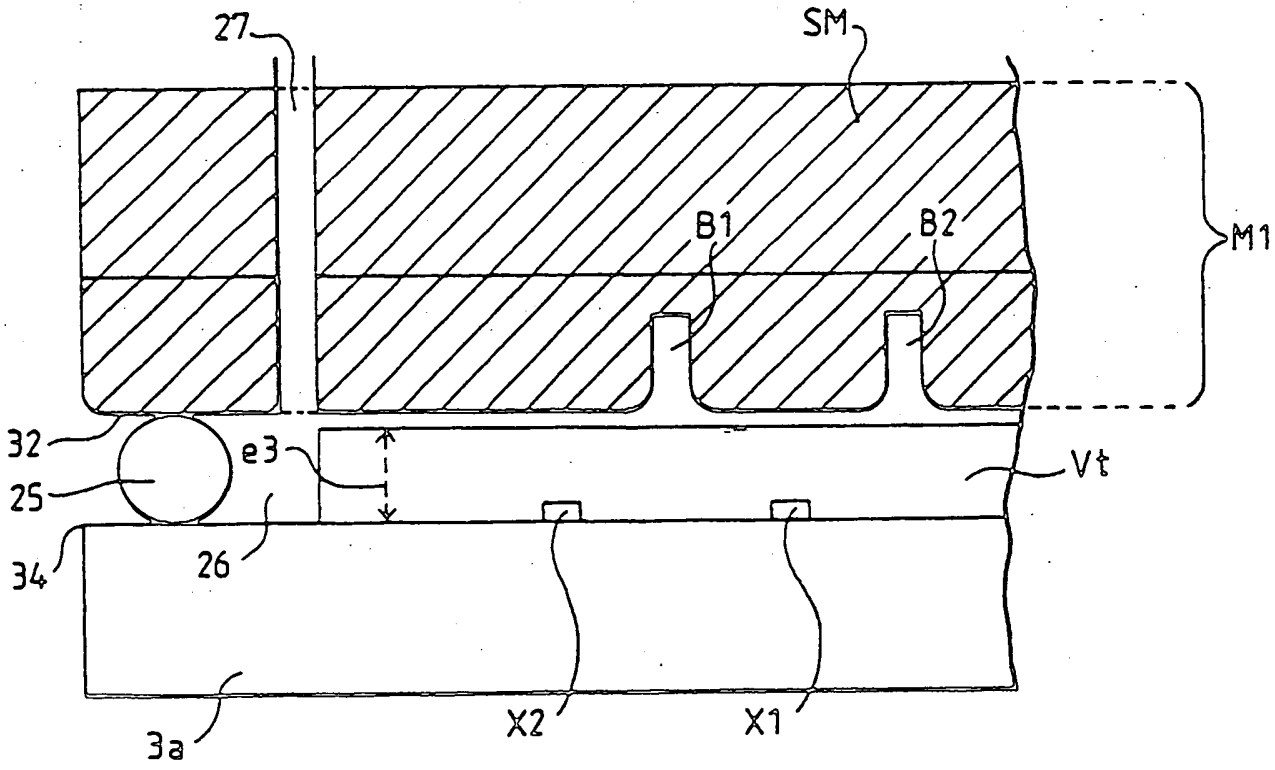
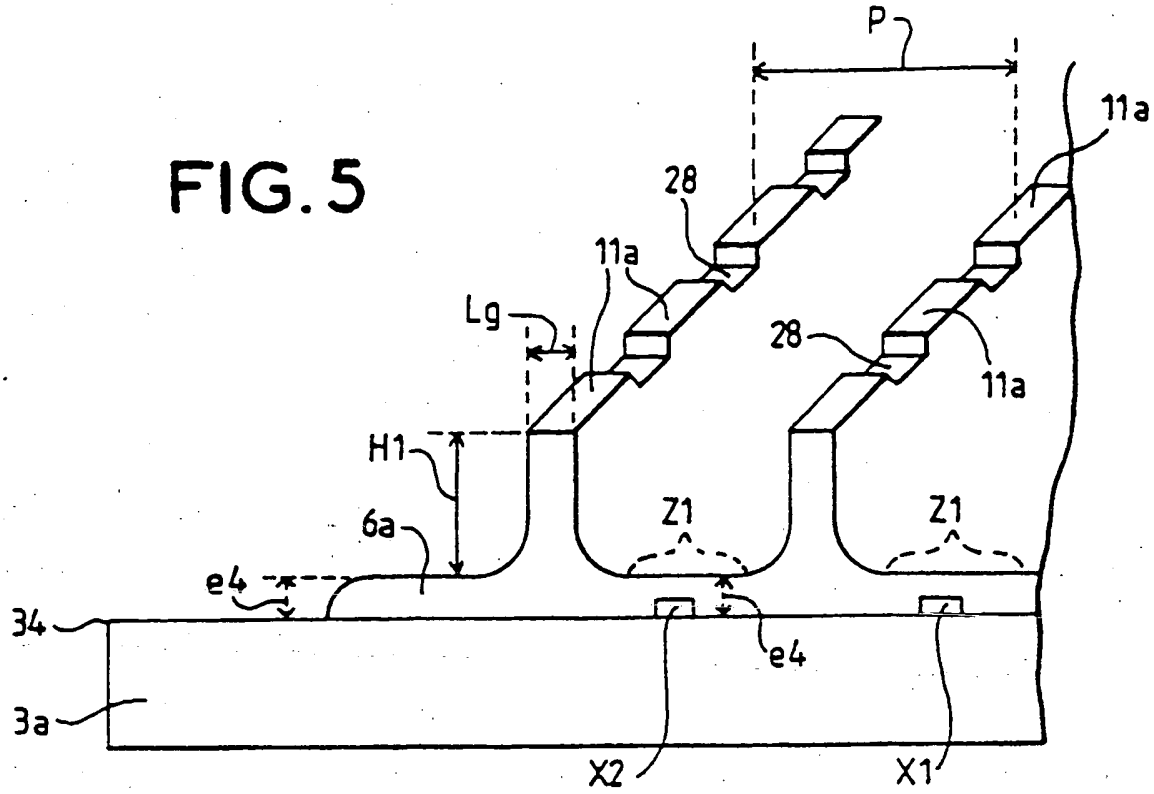



FIG.4

FIG. 5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11a
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11a
Lg
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11a
H1
6a
Z1
Z1
e4
34
e4
3a
X2
X1

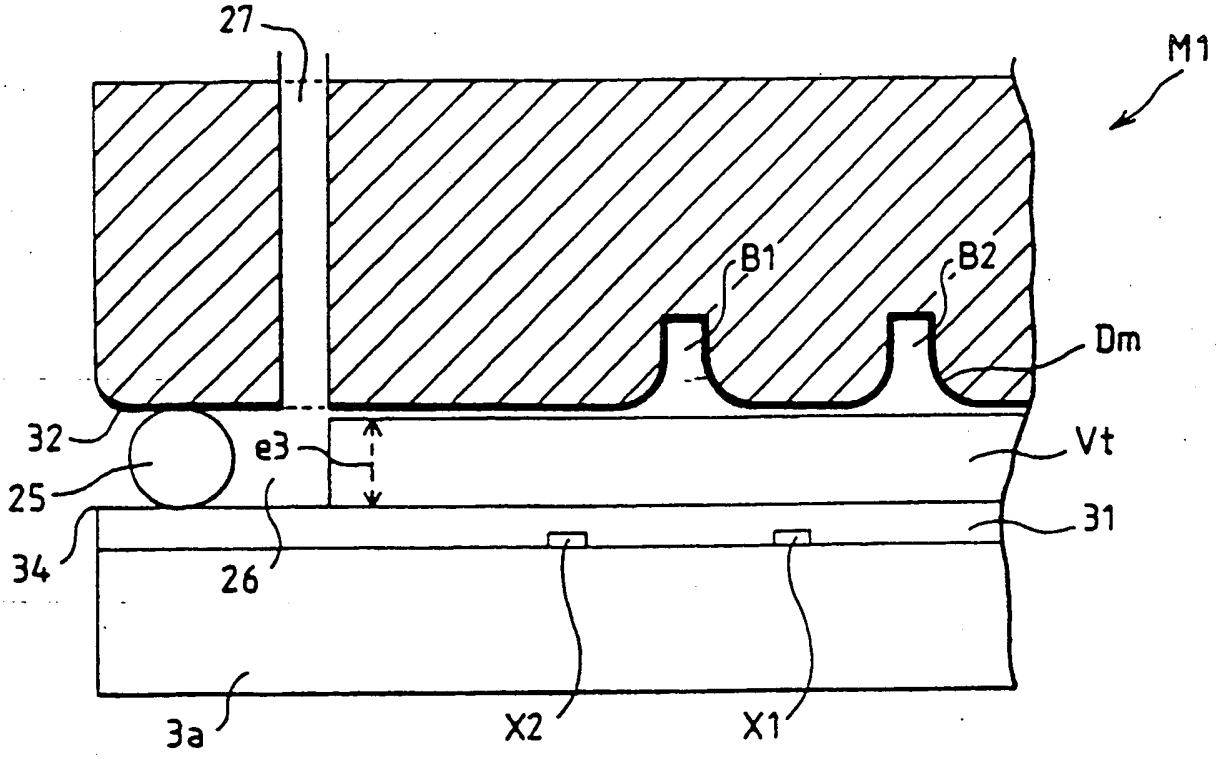
27
M1
B1
B2
Dm
32
e3
Vt
25
31
34
26
3a
X2
X1

FIG. 6

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